Federal State Budgetary Educational Institution of Higher Professional Education

National Research University "MPEI"

Laboratory work No. 2

on the course "OEVM"

CONSTRUCTION OF A CONTROL DEVICE

Completed by students:

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Team No. 6

Group A-09-19

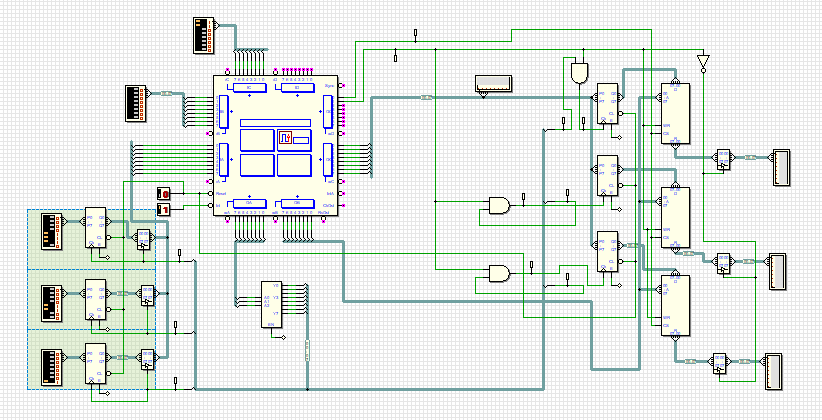
National Research University "MPEI",

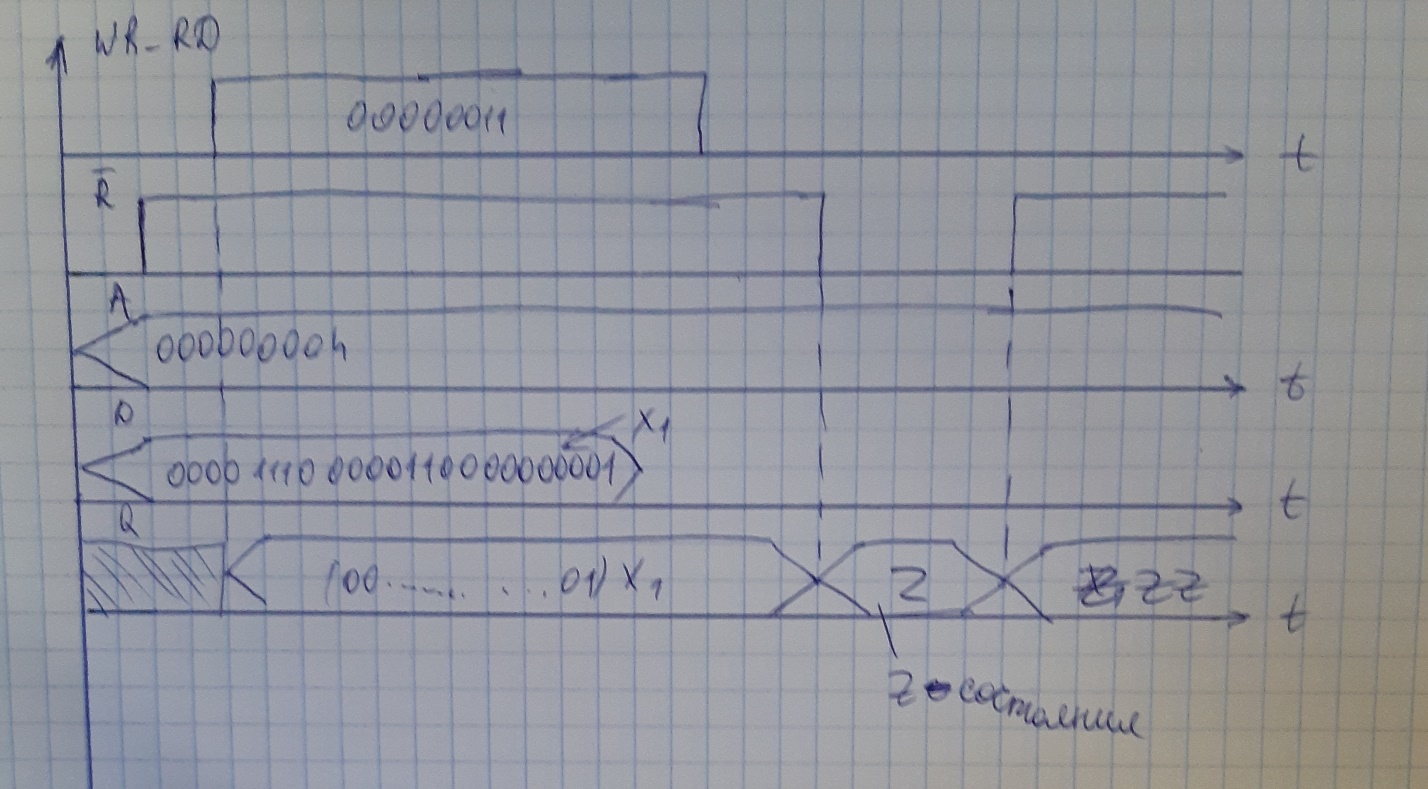
Moscow 2022

Part 1.

1. Build a circuit containing a DMC8 microcontroller and build an external memory according to the option (table 1). The memory is built on the basis of ready-made blocks (RAM) deeds. Test the circuit, make a timing diagram of reading/writing to memory.

|  |  |
| --- | --- |
| № | Число слов х Разрядность |
| 6 | 256 х 24 |

Circuit diagram with microcontroller:  


Timing diagrams:

portA EQU 00

portB EQU 01

portC EQU 02

portD EQU 03

JP START

ORG 38h

JP INTERRUPT

ORG 100h

START:

EI

INF:

JP INF

RG\_READ:

IN A, (portC)

OUT (portD), A

IN A, (portB)

OUT (portB), A

LD A, 001b

OUT (portA), A

IN A, (portA)

LD B, A

LD A, 010b

OUT (portA), A

IN A, (portA)

LD C, A

LD A, 011b

OUT (portA), A

IN A, (portA)

LD D, A

LD A, B

OUT (portC), A

LD A, 100b

OUT (portA), A

LD A, C

OUT (portC), A

LD A, 101b

OUT (portA), A

LD A, D

OUT (portC), A

LD A, 110b

OUT (portA), A

LD A, 000b

OUT (portA), A

RET

INTERRUPT:

CALL RG\_READ

EI

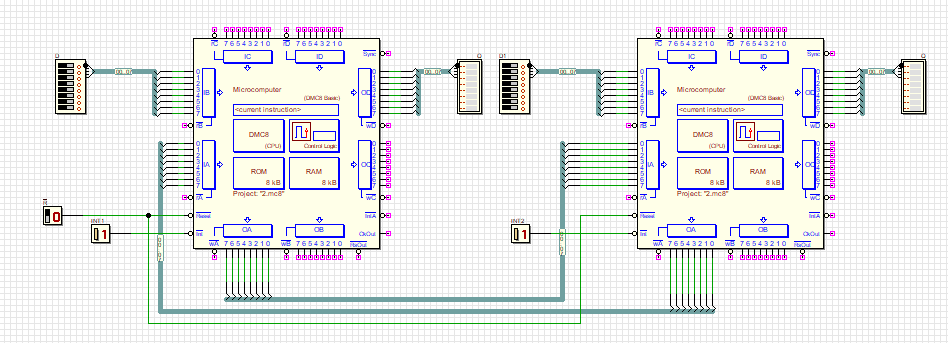
RET

**Part 2.**

Build a circuit containing two DMC8 controllers. Develop a

communication protocol between the two controllers. The communication word is 8 bits. Both controllers must be able to send and receive data from the other controller.

Scheme:



portA EQU 00

portB EQU 01

portC EQU 02

portD EQU 03

JP START

ORG 038h

JP INTERRUPT

ORG 100h

START:

EI

INF:

IN A, (portB)

OUT (portA), A

JP INF

INTERRUPT:

IN A, (portA)

OUT (portD), A

EI

RET

**Part 3.**

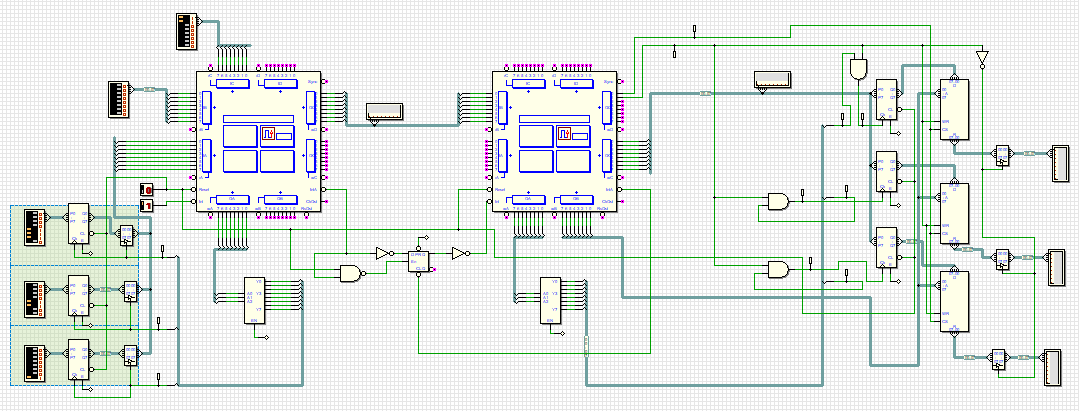
Build a circuit containing two DMC8 controllers. DMC8

must be connected using the interface developed in p.2.

The first controller has inputs for “address” and “data” in accordance with p.1,

the second controller is connected to the memory in accordance with p.1. It is required to use DMC8 (1) to read/write the memory connected to DMC8 (2).

Scheme:



Listing of the program for the 1st microcontroller:

PORTA EQU 00

PORTB EQU 01

PORTC EQU 02

PORTD EQU 03

ORG 0000H

JP START

ORG 0038H

JP INT

ORG 100H

START:

EI

INF:

JP INF

INT:

IN A,(PORTC)

OUT (PORTD),A

AND 00000011B

CP 00000011B

JP Z,WRITE

IN A,(PORTC)

AND 00000001b

CP 00000001b

JP Z,READ

EI

RET

WRITE:

NOP

;;;;;;;;;;;;;;;;;;;;;;;;;;;

LD A, 001b

OUT (portA), A

IN A, (portA)

OUT (portD), A

LD A, 010b

OUT (portA), A

IN A, (portA)

OUT (portD), A

LD A, 011b

OUT (portA), A

IN A, (portA)

OUT (portD), A

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

LD A, 000b

OUT (portA), A

nop

NOP

NOP

EI

RET

READ:

;;;;;;;;;;;;;;;;;;

IN A, (portC)

OUT (portD), A

IN A, (portB)

OUT (portD), A

;;;;;;;;;;;;;;;;;;

nop

EI

RET

Listing of the program for the 2nd microcontroller:

PORTA EQU 00

PORTB EQU 01

PORTC EQU 02

PORTD EQU 03

ORG 0000H

JP START

ORG 0038H

JP EXEC

ORG 100H

START:

nop

EI

INF:

JP INF

EXEC:

NOP

NOP

NOP

NOP

NOP

IN A,(PORTB)

OUT (portD), A

AND 00000011b

CP 00000011b

JP Z, WRITE

CP 00000001B

JP Z,READ

EI

RET

WRITE:

NOP

NOP

NOP

IN A, (portB)

OUT (portC), A

LD A, 100b

OUT (portA), A

IN A, (portB)

OUT (portC), A

LD A, 101b

OUT (portA), A

IN A, (portB)

OUT (portC), A

LD A, 110b

OUT (portA), A

LD A, 000b

OUT (portA), A

EI

RET

READ:

NOP

NOP

nop

nop

IN A, (portB)

OUT (portD), A

IN A, (portB)

OUT (portD), A

EI

RET